ECR#: P21
Tracker #: 28
Status: Ratified
Title: 3.3Vaux signal definition for compliance with PCI 2.2 (PM 1.1)
Release Date: October 1998
Impact, High
Spec Version: NLX Motherboard Specification 1.2

Summary:

Table 4.10 needs to be revised to define a pin for 3.3V Standby (3.3Vaux) on the NLX riser, necessary for compliance with PCI 2.2 (PM 1.1). To be compliant with PCI 2.2 (PM 1.1), the system must be able to provide standby power to pin 14A of the PCI connectors on the riser.

Changes Current Specification As Shown:

In Table 4.10, change the following pin definition:

Before --

Pin	Signal Name	Type	I/O	Termination
A135	RESERVED	RES	N/A	N/A

After --

Pin	Signal Name	Type	I/O	Termination
A135*	3.3Vaux	PWR	O	N/A

Add footnote below Table 4.10 on page 43:

* Pin A135 is rated at 2A.